SOCIÉTÉ DES INGÉNIEURS DE L'AUTOMOBILE

White Paper on Open Source Hardware

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ABSTRACT

This White Paper explores the evolving landscape of automotive electronic architectures, currently in transition towards software-defined vehicles, and focuses on the potential of open source hardware, particularly RISC-V. It analyzes the challenges and opportunities presented by this shift, emphasizing the need for innovation in electronic control units and the role of academic and industry collaboration. The paper, also, examines the strategic importance of RISC-V and open source hardware in fostering European sovereignty in semiconductor technology and the broader implications for the automotive industry.

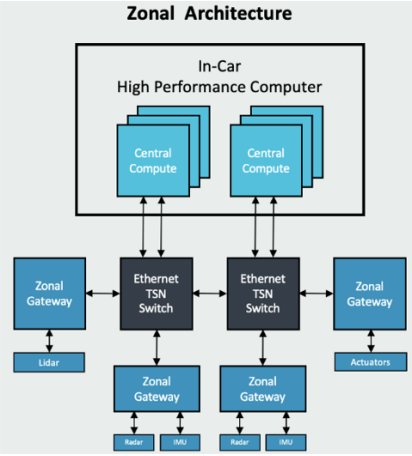
1. Automotive Context

1.1. SIA EXPERT COMMUNITY

Expert committees and working groups are one of the cornerstones of operations that the *Société des Ingénieurs de l'Automobile* (SIA) covers, sharing knowledge and needs of the automotive industry on non-competitive topics.
Since the beginning of 2024, the SIA expert community and its working group on electrical and electronic architecture have complemented their work by addressing new issues given by the revolution of introducing Software-Defined Vehicles. This working group strengthens itself with the contribution of new academic experts from CEA, INRIA, and CNRS to enrich exchanges and address perspectives and proposals from the field of applied research, as well as to strengthen the close link with the world of higher education. The ambition is the proposition of agile and time-limited working groups to address targeted technical topics and to document this work.

1.2. TOWARD THE SOFTWARE-DEFINED VEHICLE

Among the issues related to software-defined vehicles driven by the shift from mechanical engineering to software and the digitalization of the vehicle, we decide paradoxically to create a working group analyzing needs and future impacts on electronic control units. The expected results are to identify where current hardware research and academic activities can bring value on hardware component of electronic control unit.
The McKinsey report "Automotive software and electronics 2030" [8] exhibits the fact that electrical and electronic in vehicle architecture faces a major evolution to move from distributed to centalized architecture. Centralization comes along with a separation of hardware and software, supported by a layered architecture with clear hardware abstraction that allows domain virtualization. The connection to local safety and real time controller is performed through high speed and deterministic Ethernet backbone.
The central computer evolves into a High Performance Computer (HPC), requiring increasingly higher computing performance while also managing its electrical consumption. For example, the ADAS virtualized domain on the central computer, which performs data fusion for environment reconstruction using local distributed perception sensors, requires specialized acceleration, particularly for AI accelerators.
The HPC architecture moves towards the hardware architecture of scientific HPC, including many-core processors, accelerators, and cluster organization. Additionally, the local real-time safety controller, also, includes hardware accelerators for communication, security, efficient I/O, and perception control, thereby improving computing efficiency and energy consumption.
The Huawei survey document “Intelligent Automotive Solution 2030” [3] emphasizes the evolution towards a central computing and



An example of a zonal architecture

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communications architecture for software-defined vehicles. This involves shifting the profit model from hardware to software and relying on standard ICT technology and standardized computers.

The E/E architecture consists of a central computing platform, zonal control, and high-bandwidth in-vehicle networks, as illustrated in Figure 1 [1]. The central HPC performs several thousand trillion operations per second (TOPS), ensuring trustworthiness and functional safety. Central computing plus zonal control offers stability and functionality scalability. Mastering hardware design and computing performance remains a key expertise ensuring the expected performance of future electronic control units.

1.3. TOWARD HARDWARE INNOVATION

The Strategic Research and Innovation Agenda (SRIA) [4] of Electronic Component and Systems (a.k.a., ECS, developed by the following associations AENAS, EPoSS, and Inside) related to the semiconductor industry, addresses cross-sectoral foundations on component modules and systems integration technology layers to increase performance and reduce power consumption.
The SRIA describes challenges to be solved in micro and nanotechnology relevant to computing ressource for Software Defined Vehicule as follows:

- Challenge 1: "Advanced computing, memory, and in-memory computing concepts" identifies technology issues (e.g., CMOS, FDSOI, FinFET, for transistors, etc) but also architecture topics for memory access and heterogeneous architecture to deliver better performance and reduce power consumption.
- Challenge 2: "Novel devices and circuits that enable advanced functionality" tackles devices for new sensing and actuating concepts. The related innovations on main components embedded in Edge computing are processors with energy efficiency, acceleration (for AI and other tasks), Data Processing Units (DPUs - collecting and processing data), memory and associated controllers (low power), embedded microcontrollers, and power management.

The automotive sector is a driver of innovation using solid know-how in embedded systems and extending it with high perfomance computer device. For instance, this is visible through the "European Processor Initiative" (EPI) started in 2020. The ECS SRIA explicitly references innovation around RISC-V and Open Source Hardware as key ingredients to keep Europe in race.
The focus of the working group is to identify trends and innovations in the field of hardware by analyzing the emergence of open source hardware, strongly supported by the academic world and identified as a potential vector of innovation for the automotive industry.
The members of the SIA working group therefore decide to document strengths and weaknesses of this emerging field by applying it to the new ecosystem and assessing the impacts around the RISC-V initiative. In a very

[1] https://www.eetimes.eu/unveiling-the-transformation-of-software-defined-vehicles

active field with daily announcements around RISC-V solutions, it seems important to us to measure the potential for its involvement in future electronic architectures and automotive systems. This is especially important as ECS experts propose a RISC-V roadmap [5] and potential for future automotive RISC-V development in Europe in February 2024 to support the evolution of automotive architecture.

2. RISC-V CONTEXT AND OPEN SOURCE HARDWARE

2.1. A BRIEF HISTORY OF RISC-V

The RISC-V (Reduced Instruction Set Computing, Version 5) project is started in 2010 by Professor Krste Asanovic and his team at the University of California, Berkeley. Inspired by the impact of open source software like Linux, which had revolutionized the computing industry by fostering collaboration and standardization, the primary motivation behind RISC-V is the creation of an open and standardized instruction set architecture (ISA) that could be freely used, modified, and integrated in processors and computing systems, ranging from deeply embedded systems to higher performance computing servers.
After decades of consolidations leading to an Intel/ARM quasi-duopoly on processor architectures, the European sovereignty concern is raised when ARM is acquired by Soft-Bank in 2016. The situation escalated further in Europe when NVidia attempted to acquire ARM in 2020, potentially limiting Europe's ability to innovate and compete in the global semiconductor market. Similarly, the Chinese industry, especially Huawei, is targeted in 2019 by an export ban on American technologies in ARM cores.
At that point, RISC-V had demonstrated its viable potential as an alternative to Intel and ARM cores, while remaining independent from both financial and geopolitical fluctuations.

2.2. ECOSYSTEM AND GOVERNANCE

Since 2010, the RISC-V ecosystem has grown into a global community of both public and private research and development organizations, covering the whole range of activities from HW and SW-dedicated research, hardware design for processor RISC-V cores or dedicated accelerators, processor or SoC design and fabrication, hardware devices manufacturing, hardware-specific software development, and systems integration.
In 2015, the RISC-V International Foundation [2] is established to standardize the ISA and extensions, synchronize with other initiatives, and animate the ecosystem notably with 3 yearly RISC-V summits in Northern America, Europe and China. Most members are from United States or China.

The OpenHW Group[3] (soon to be hosted by the Eclipse Foundation), as well as the CHIPS Alliance[4] (hosted by the Linux Foundation) focus on the development of open source RISC-V cores, IPs and software tools. Several European organizations contribute to the OpenHW Group (notably ETHZ, CSEM, GlobalFoundries, Siemens, CEA, Thales, Kalray). The Linux Foundation-hosted RISE project (RISC-V Software Ecosystem) dedicates to supporting software layers.

2.3. OPEN SOURCE HARDWARE

Open source hardware [5] represents a transformative approach to hardware development, drawing inspiration from the success of open source software. Its adoption is, however,

[2] https://riscv.org/
[3] https://www.openhwgroup.org/
[4] https://www.chipsalliance.org/
[5] https://www.oshwa.org/

slower than for open source software because of the traditional closed IP business model.
While the RISC-V instruction set architecture (ISA) is open and freely available for use, modification, and distribution, the RISC-V licence allows integration into both free and commercial products. In fact, the implementation of a RISC-V-based system usually involves many additional steps that involve additional costs:

- from the RISC-V ISA to a working RISCV Core design (HDL) - although several open source cores are available (e.g. EPFL's PULP platform [7]), higher-performance cores are more often commercial.
- from a RISC-V core to a funcional SoC RTL design, many additional IPs (Intellectual Property, i.e. modular building blocks) are required such as memory interfaces, caches, various accelerators such as crypto, GPU or NPU (Graphic and Neural Processing Unit), they usually involve a license fee;
- fab and foundry costs to manufacture the actual SoCs, including acess to a PDK (Process Design Kit);
- although several compilers and operating system stacks already support the RISCV ISA (e.g. the GCC compiler collection, the Linux and FreeRTOS operating systems), they show variable maturity levels, so that many performance optimizations or specific drivers require costly additional developments.

Although the RISC-V ISA is free, a RISCV system is certainly not. Many additional components are available in the open source HW/SW ecosystem, but often restricted to lower performance or lower maturity, so that a high-performance RISC-V based system remains an IP-intensive product.
However, after decades of developments under heavy Non-Disclosure Agreement (NDA) rules, the availability of a de facto standard, freely accessible ISA specification, together with several reasonable performance reference open source hardware implementations, and supportive of open source software stack, is a major overhaul in the business model, and it enables a whole new world of collaboration opportunities. RISC-V has become the de facto common language for open collaboration on nondifferentiating hardware IPs.
In the automotive domain more specifically, collaborations might take several forms like EU-funded collaborative projects like the CHIPS-JU supported project RIGOLETTO, or the Quintauris joint venture. Established in 2022 with support from Thales, STMicroelectronics, NXP Semiconductors, Robert Bosch GmbH, Infineon Technologies AG, Nordic Semiconductor ASA, and Qualcomm Technologies, Quintauris[6] focuses on developing RISC-V based microprocessors mostly for the Automotive industry.

3. Bussiness model behind open source

The maturity of open source hardware increases fast, given that its growth is based on accelerated collaborations between academic and industrial communities thanks to 3rd party funding. Moreover, we consider that the RISC-V based microprocessors for the Automotive industry are, today, between the first two stages of the business model development as defined by L. Thomas in [9]. Indeed, preparing its business plan within this context requires anticipating the evolution of business models associated to an open source hardware as described in Figure 2. Based on this evolution, we discuss below arguments in favor of adopting RISC-V based microprocessors within the French and European Automotive industry while discussing how to mitigate potential risks. Moreover, this evolution is possible under the hypothesis that a dy-

[6] https://www.quintauris.eu/

namic ecosystem is created, following examples from open source software like Unix or Red Hat.

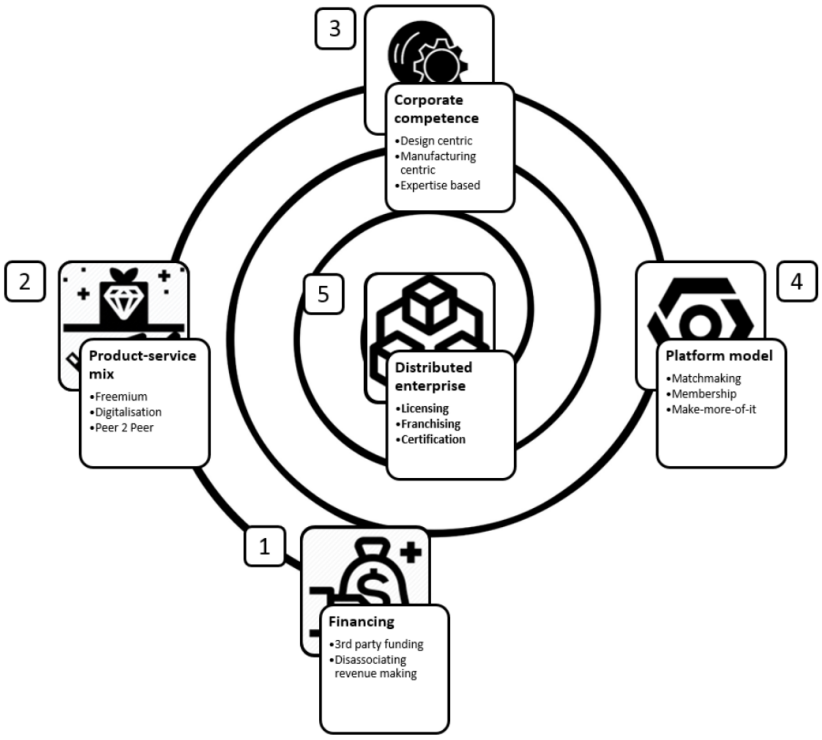
- Advantages
  - Reduced development cycle with an increased industrial acceptance as one may start with commonly agreed technologies. This is the most expected and, probably, the most wanted advantage by automotive industry actors that support open source hardware.
  - Consolidation of common understanding and practice in integrating safety and security concerns as, usually, open source hardware achieve their technical maturity together with a list of common rules/technical choices that could support certification and/or normalisation (common feature for the last stage of development).
  - Increased shared value is one side effect of developing a community around a topic, usually built from Stages 1 to 4 during the evolution of the business model. The Automotive electronic and software industry is facing a value crisis that could be solved during this evolution as an open source (software or hardware) community requires healthy rules against non-democratic choices within the gouvernance. Transparency, reproducibility and collective decisions, usually, drive open source (software and hardware) communities and we expect them to propagate if and when the fourth stage is achieved for RISC-V based microprocessors within the Automotive industry.
- Risks
  - Lack of differentiating features within the products could raise concerns if all industry actors share exactly the same hardware - this risk seems a less important concern today as some chip vendors do have the monopole on same market segments, e.g., GPU indicating that hardware is too far from customers with respect to other markets (personal computers customers may compare products based on the hardware differences).
  - Loss of access to previously shared technology advances - this risk could appear according to geographical regions as associated to lack of chip vendors in France and Europe. Mitigating this risk is done during the first stage of the business model and it requires important 3rd party funding to be increased.
  - Lack of anticipating the required legal protection - this risk is associated to industry and academia actors when open source categories are not well known, especially, contaminating properties.

4. SWOT PRESENTATION

As introduced in section 1.3, the impact of the open source RISC-V ecosystem on the automotive industry is analyzed using the Strength, Weakness, Opportunity, and Threat (SWOT) technique.

The open source RISC-V ecosystem leverages the open instruction set to strengthen the core, memory interconnect, and related accelerators, as well as related software development tools (compiler, simulator, etc.) through initiatives such as the OpenHW Group and Open Alliance[7]. Differentiating features such as safety and overall architectural performance are intended to be managed in derived commercial offerings. Consequently, the scope of the study for the RISC-V SWOT analysis is limited to RISC-V component use cases such as microprocessors, microcontroller computing and memory architecture, hardware acceleration with vectorized instruc-

[7] https://riscv.org/alliances/



Evolution of business model for open source hardware-based products [9]

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tions, Graphical Processor Units (GPUs), and Artificial Intelligence accelerators.

4.1. STRENGTHS

The strenghts of the open source RISC-V ecosystem are seen as follows:

- Open Hardware Collaboration Model: The open source model reduces development costs by sharing designs and resources, accelerates innovation through open collaboration and the ability to connect with the academic research world, promotes transparency in development by building trust.
  It also facilitates the sharing of needs within the community and developers to create designs that meet needs, ensures the sustainability of available and open solutions.
- Opening market for hardware accelerators: The RISC-V open source model facilitates the development of specialized IPs that implement instruction extension mechanisms such as vector instructions, but also by relying on low-footprint and low-power of basic RISC-V core implementations.
  This enables performance improvements for customized needs such as cryptographic calculation or communication router, as well as optimizing performance for complex calculations, particularly on AI accelerators, while prioritizing the reduction of energy consumption brought by the characteristics of the RISC-V instruction set.
- Reinforce research and innovation: The RISC-V open source model and its ecosystem promote free access to open resources facilitating experimentations and the development of innovations.
  The open source model favored by researchers encourages the sharing of results and the acceleration of scientific advances, allowing academic research networks to be enriched with concrete and shareable elements.

Ultimately, it helps bridge the gap between the research field and industry by sharing common assets.

- Facilitate hardware-software co-design: The extensibility of the RISC-V instruction set allows for the adaptation and optimization of software for dedicated hardware, enabling gains in performance and energy consumption.
  To support this, the RISC-V ecosystem includes commercial tools and research prototypes that automate these developments through hardware code generation, compiler extensions for these new instruction sets, and features for evaluating gains and comparing alternative solutions.
- Financial support from the European Commission and national bodies: The European Commission, through the Chip-JU initiative[8] aims to strenghen the European secomiconduction by allocating a budget of 15,8 billions euros.
  It includes a portion on the introduction of a roadmap for European sovereignty in hardware and open source software. Specifically, calls for development tools, the creation of IP, and an open hardware ecosystem around RISC-V are co-funded by national states and the Commission.
  For automotive industry a dedication action and budget line related to SDV and led by DG CONNECT[9] is existing that covers also software infrastructure.
  Similarly, the EuroHPC initiative[10], aiming to promote the development of world-class supercomputers, proposes specific actions on the RISC-V ecosystem, particularly through EPI (European Processor Initiative) calls for HPC, with one of the targets being embedded systems.
- Competence and Hardware IP Design Ecosystem in Europe: Europe is home to several major players in the field of digital electronics design and manufacturing, key players in the automotive industry (ASML, Infineon, ST Microelectronics, NXP Semiconductors...), as well as leading fabless companies (Soitec, ARM, IMEC, Bosch, Thales...).
  It has a powerful ecosystem with partnerships between universities, research centers, and industry, supported by European research programs that promote innovation and knowledge exchange.
  Finally, it integrates a pool of qualified talents thanks to the excellence and diversity of top-tier European training programs specialized in electronics.

4.2. OPPORTUNITIES

The opportunities of the open source RISC-V ecosystem are seen as:

- Diversification in case of acquisition of ARM by a major semiconductor player: The current quasi-monopoly of ARM core technologies in the embedded computing markets poses a risk of strong dependency, reduction of supply, and therefore an increase in prices, as well as potentially restricted access to technology in the event of consolidation with a powerful semiconductor player, as initiated by NVIDIA in 2023.
  The adoption of RISC-V technology by companies provides guarantees thanks to its open ecosystem and the multitude of cores solutions and tools exploiting the basic open source technology, which offers flexible alternatives and a great diversity of solutions.
  Moreover, the research programs and startups using this technology are driving the rapidly growing market of AI accelerators and the Internet of Things (IoT).
  This diversification at the heart of innovation is a real opportunity for semiconductor companies.
- Collaboration with China: Collaboration with China accelerates innovation while

[8] https://www.chips-ju.europa.eu/

[9] https://digital-strategy.ec.europa.eu/en/policies/digital-vehicle-ecosystem

[10] https://eurohpc-ju.europa.eu/index_en

reducing development costs due to the large number of developers involved in the development of this technology.
A typical example is the open source XiangShan project initiated by the Academy of Sciences to create a high-performance open source RISC-V processor, which receives support from numerous industrial companies. The Beijing Institute of Open Source Chip, a non-profit organization, is created to support the development of cores on an open GitHub[11], whose performance and efficiency are recognized in the field of HPC research[6].
Research and development partnerships between academic institutions thus promote the exchange of knowledge and skills.

- Opportunities for French and European players: The semiconductor market using RISC-V cores allows new or established design companies to benefit from greater independence, rapid innovation, and infrastructural and collaborative support with research.
  The sectors of artificial intelligence, cybersecurity, and the Internet of Things (IoT) are very active, offering opportunities for new, high-performance, and efficient specialized IPs.
  Additionally, the use of RISC-V cores as an alternative to traditional architectures for established SoC or IP providers is also an opportunity for independence from ARM technologies.
  Access to these technologies is also facilitated for small structures with the free technologies and tools available in the ecosystem.
- Efficiency Brought by Technology: The RISC-V instruction set is designed to be simple, regular, and efficient, with reduced encoding that minimizes the number of execution cycles. Its reduced and scalable instruction set decreases the complexity in core design and promotes efficiency with a small footprint.
  Additionally, the extensibility of the instruction set allows for the completion of these cores by optimizing repetitive operation sets as needed.
  For solutions requiring more complex calculations, optimizations are possible with vector operations or specific operators, minimizing the number of cycles.
  For example, the manufacturer SiFive[12] claims 30-40% better power efficiency and a smaller size on its general purpose computing core.
- Contribution of Safety Expertise to the Open Hardware Ecosystem: The knowledge from the European industrial and research ecosystem in the automotive and industrial sectors, particularly chip designers accustomed to developing SoCs dedicated to these critical, safe, and secure applications, is a real asset for strengthening open RISC-V solutions.
  Taking these constraints into account enhances the utility of available open source solutions but also allows differentiation in derived commercial solutions.
  This expertise is a true asset of the European semiconductor industry to boost innovation and cover the market for specialized accelerators.
- Designing software stacks and tools: The open and royalty-free architecture of RISC-V instructions promotes the development of both free and commercial tools for software development on these cores.
  Additionally, the academic and open source developer ecosystem is very active in these activities, allowing for more freedom in development and customization of RISC-V solutions to introduce innovations.
  Compilers, operating systems like Linux or FreeRTOS, and simulators are freely available, enabling rapid and cost-effective development, as well as the development of specific extensions supported by tool adaptations.

[11] https://github.com/OpenXiangShan

[12] https://www.sifive.com/

This open ecosystem is a true facilitator for development and opens up numerous opportunities for the development of software stacks for embedded systems such as automotive, while also nurturing and maintaining an open source ecosystem more easily.
Typically, most Linux distributions such as Ubuntu, Fedora, etc., support RISC-V cores, and evaluation boards based on RISC-V cores from the openHW Group[13] are available for software development.

- Chiplet as a catalyst for this technology: The emergence of chiplets, driven by the standardization efforts of UCIe[14] (Universal Chiplet Interconnect Express) for rapid interconnection interfaces between hardware IPs to compose chiplets, presents a real opportunity to support the development of RISC-V technologies.
  This standardized and open interoperability boost the integration of specific IPs, particularly AI accelerators from various sources, in combination with high-performance memory architectures and general-purpose cores and interconnects.
  These chiplet solutions are able to cover applications requiring high performance, such as those needed in HPC for SDV deployment.
  This new modularity also allows for a scalable diversity of performance needs, enabling the use of innovative solutions based on RISC-V.

4.3. WEAKNESSES

The weaknesses of the open source RISC-V ecosystem are seen as:

- Emerging RISC-V Market: the RISC-V SoC market is estimated at USD 0.92 billion in 2024[15], primarily distributed in Asia and mainly in the IoT market. This represents only a very small part of the global SoC market[16], which is valued at over USD 350 billion, with the automotive market accounting for approximately USD 10 billion[17], still seen as a niche market compared to cunsumer market.
  Although a strong growth of over 30% is predicted by 2030 for RISC-V, current penetration in the automotive field is very low, where Renesas is seen today as the only historical supplier distributing a RISC-V core microcontroller[18].
  However, a number of historical players comes together to work on RISC-V adaption for automotive in Quintauris. Other emerging players in the automotive field distributing solutions include SiFive, ANDES, etc. (non-exhaustive list).
  Most of the solution available are Microcontrollers (MCU) mostly designed for IoT market whereas performance processors are still under design (with the exception of SiFive as pionner in this new performance market).
- Reluctance of Automotive Industry Players: the automotive industry is conservative, mainly due to the reliability and safety/security constraints essential to mitigate risks to people and financial risks.
  Changing processors and the associated tooling requires human investment, as well as a solid validation set demonstrated through significant experience feedback. The entire value chain of the automotive industry must be convinced, with decision-makers actively participating in technology choices.
  Additionally, although open source software is present in automobiles mainly in the infotainment domain, open source

[13] https://www.openhwgroup.org/core-v-devkits/
[14] https://www.uciexpress.org/
[15] https://www.mordorintelligence.com/fr/industry-reports/risc-v-tech-marketes
[16] https://www.mordorintelligence.com/fr/industry-reports/system-on-chip-soc-market
[17] https://www.mordorintelligence.com/fr/industry-reports/automotive-semiconductor-market
[18] https://www.renesas.com/en/products/microcontrollers-microprocessors/rz-mpus/rzfive-general-purpose-microprocessors-risc-v-cpu-core-andes-

hardware is a new model still maturing with no clear governance and asociated business model.
However the automotive electronic supplier industry identifies an interest for RISC-V technologie, and the short-term penetration this technology seems more feasible in security or AI accelerators, a new and rapidly growing market.

- Current computing performance: Unlike x86 processors, ARM and RISC-V cores have simple, scalable, and reduced instruction sets, which give them better performance per watt.
  ARM processors are widely deployed in large ecosystem including derived SoCs for automotive applications. ARM processors are designed to deliver performance with low power consumption, and notably, the latest generation of offers performance gains of around 30% and 50% in terms of power consumption compared to the previous generation (ARMv8)[19].
  RISC-V cores are designed to be competitive in terms of power consumption but are still too nascent to be competitive in performance with ARM.
  A recent scientific publication [1] from 2024 based on open source implementations highlights that the RISC-V architecture consumes fewer watts than the ARM architecture but is less performant, ultimately generating more dissipated energy with longer execution times.
- Non-standardized memory model: Only the instruction set of RISC-V processors is open and standardized. However, the CPU architecture and the associated memory model, such as the definition and optimization of memory buses and interconnects, the mechanisms implemented in the pipeline, memory banks and their various optimizations (DRAM, HBM, Scratch PAD, Flash, etc.), are all crucial for the execution performance of a processor.
  This performance optimization also covers the management of memory banks to access accelerators, which is critical for AI and cryptography accelerators.
  This memory model is competitive and is not addressed as a priority by open source hardware projects, and is therefore considered a closed source, which is a weakness for the deployment of high-performance RISC-V solutions.
- Maturity Level on Reliability: Complex SoCs developed for the automotive market integrate mechanisms to meet safety and security requirements, such as Memory and I/O Protection Units (MPU, IOMPU), Memory Test Units (MTU), lockstep, Built-in Test modules, Safety Management Units, End-to-End protection on bus and memory, debug protection, Hardware Security Modules (HSM), Trusted Zones, security instruction sets, etc.
  Open source implementations do not integrate these features, which are mandatory and differentiating for SoC providers. The MCUs currently available on the market, primarily targeting the IoT market, do not contain all these features. Additionally, the application of ISO26262-Part5 on hardware must be demonstrated on these components to cover the highest safety integrity level (ASIL-D).
  Therefore, SoCs need to mature to meet automotive needs and provide guarantees on the reliability of components in operation.
- Incomplete solution for AI accelerators: The solutions developed for hardware accelerators are mostly managed in open source hardware by academics or startups, all in a competitive way. Furthermore, there is no emerging solution for an open hardware GPU.
  Vector extensions are available for RISC-V in the standard, but it also offers specific extension mechanisms that allow for specific acceleration implementations. This makes it difficult to unify across various implementations or application pur-

[19] https://newsroom.arm.com/blog/armv9-cortex-x925-cpu-performance

poses, and the same is true for software stack drivers.
Moreover, some commercial tools exist to automate hardware customization and software compiling in the context of instruction customization. However, generally, there is a gap in supporting the complete development of accelerators, typically AI acceleration, from high-level design of neural networks, for example, to implementation in the target with RISC-V specificities.

- Risk on emerging solutions for HPC: As mentioned in section 4.2, collaboration with China, particularly on the HPC work of the XiangShang project (mainly targeting cloud needs), is both an opportunity and a risk.
  Indeed, the geopolitical situation between China and the West, particularly the United States, could lead to embargoes or restrictions, as discussed today by the American Congress regarding IRTA rules and RISC-V

4.4. THREATS

The threats of the open source RISC-V ecosystem are seen as follows:

- The business model around open hardware is unclear: It is perceived as complex and uncertain because, unlike software, hardware requires different skills and significant investments to design and produce electronic components. The economic model is not yet established in this field, especially in the automotive industry where the value chain is very hierarchical and structured. Responsibility, critical development constraints, and economic competition are determining factors in the choices of stakeholders, which seem difficult to value in an open source context. Communities for industrial exploitation are fragmented and still in the process of structuring to this day.
- Competitiveness of European players compared to the rest of the world: Compared to Europe, investments in research and development are more aggressive and substantial in the United States and China, where these states have massive policies supporting the electronics industry.
  Access to capital is more favorable in the United States due to the more developed management of venture capital firms, and the public financial power of the Chinese state is omnipresent in its support for the industry as well as in universities.
  On the other hand, in the United States, universities play a crucial role in startups with dedicated partnership programs, mentoring, and access to resources, with a culture of innovation and risk-taking that is less present in Europe.
- Unbalanced public support compared with the United States and China : RISC-V technology becomes a strategic issue for China and the United States, both of which are investing heavily.
  For China, it is an opportunity to reduce dependence on Western technologies, with major companies like Alibaba investing in this technology as described in this article [2]. Additionally, the strong support from the Chinese state for education and numerous universities is evident through the strong positioning of the Chinese Academy of Sciences[20].
  In the United States, where RISC-V technology is invented at the University of Berkeley, there are many electronics startups using RISC-V, such as SiFive, a pioneer in RISC-V processors, which already has a significant global market.
  Major American companies like Google, Qualcomm, and NVIDIA are investing heavily in RISC-V, and leading research laboratories are also working on RISC-V-related projects. The CHIPS Act provides strong support, with several hundred of billion dollars allocated to the semiconductor industry, including a por-

[20] https://english.cas.cn/newsroom/cas_media/202305/t20230529_331088.shtml

tion specifically for RISC-V, particularly in Tech Hubs, as well as the RISC-V Foundation to support its research.
These dynamics show that RISC-V has become a new front in the technological competition between these two countries.

- Sovereignty for open source and ITAR rules: In the United States, the government is currently examining the potential risks associated with China's use of RISC-V. Members of Congress have expressed concerns about the possibility that China could use this technology to circumvent restrictions on the export of advanced chips.
  The U.S. Department of Commerce is considering measures to limit China's access to this technology. In particular, ITAR regulations on the control of the manufacture, sale, and distribution of defense and space-related items and services defined in the munitions list could be subject to export controls.
  Additionally, this introduces an additional risk to the governance evolution around RISC-V and its associated ecosystems.
- Rare and Valuable Skill: The development of semiconductors requires advanced skills in digital and analog design, simulation, and verification methods.
  Acquiring these skills to be proficient takes many years of experience. In this context, there is a high demand for talent in this industry and in RISC-V, particularly driven by the growth of the AI field where companies are investing heavily and competing in the markets.
  Recruting these profiles requires time and can also constitute a strong call for resources from the academic field, influencing research programs.
- Attention point on the possible introduction of Trojan Horse in hardware IP: The open source model can be an entry point for the introduction of malicious modifications or hidden channels in the hardware IP code.
  These modifications compromise reliability or introduce security risks that are potentially difficult to detect due to the complexity and amount of code required to implement a complex IP.
  However, this risk can be mitigated by implementing vigilance and a solid and reliable governance structure within the hardware ecosystem, as well as by establishing thorough verification processes, including formal methods when applicable.
  Note, that for the automotive industry which involves critical applications, the verification processes are very mature and reliable among semiconductor manufacturers.

5. Recommandations

The introduction of RISC-V (and accelerators) with the open source hardware model promotes sovereignty and market resilience against the risk of concentration on a single architecture. This accelerates the development of solutions through collaboration on non-competitive topics (runtime software, tools, and components) as a base solution (to be enriched, optimized, etc.) for commercial exploitation, while also accelerating innovation through collaboration with the academic world and the entire ecosystem.
Low-end MCU solutions are available, primarily targeting the IoT market, but more complex solutions are emerging, allowing expansion into other areas.
The working group therefore recommends supporting and getting involved in R&D activities around RISC-V for the automotive sector and engaging in the ecosystem to facilitate the maturation of solutions. There is not only a technical challenge for MCUs to support designs compatible with automotive safety constraints, but also a challenge for heterogeneous multi-core/many-core architectures integrating accelerators to meet the needs of embedded HPC for SDV.
There is also a place for healthy competivity

on performance of the processors where the RISC-V can gain a future market by producing alternative solutions with current dominant computing and IA accelerators solutions.
The RISC-V market is very active with many new announcements every week, far beyond the automotive market. It seems important that everyone closely follows these advances and adopts a progressive approach by creating, for example, a group to determine opportunities based on specific needs (such as accelerators) and get involved in standardizing solutions for the automotive sector.
However, it is essential to ensure European sovereignty over solutions within the ecosystem to maintain independence in an uncertain geopolitical context.

6. Conclusions

The adoption of RISC-V and open source hardware presents a significant opportunity for the automotive industry to enhance innovation and maintain technological sovereignty. By leveraging collaborative efforts and academic research, the industry can address the challenges of modern electronic architectures and accelerate the development of high-performance, energy-efficient solutions. In the medium term, strategic involvement in RISC-V initiatives will be crucial for ensuring European competitiveness and resilience in a rapidly evolving market.

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