TITLE : SDV an Open-Source Hardware: A Perfect Match for Innovation

Liliana Cucu-Grosjean, INRIA

Philippe Cuenot, Aumovio

Etienne Hamelin, CEA-LIST

The authors would like to thank **Christian Fabre (CEA)**, **Olivier Sentieys (INRIA)** and **Albert Cohen (Google)** for their valuable time dedicated in sharing their opinion and vision on the open-source hardware topic

November, 12th 2025

Scope of the WG study

Identify where **current hardware research and academic activities** can bring **value on hardware component** of electronic control unit **for SDV needs**

SWOT analysis on open-source hardware

Agenda

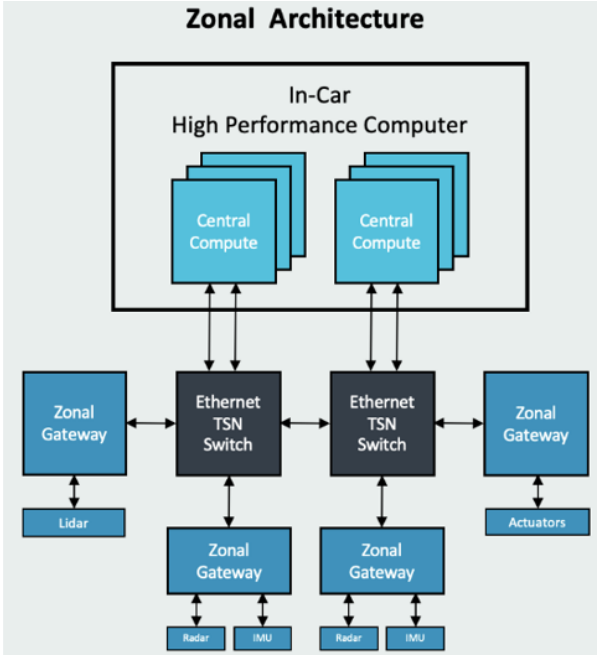
- Automotive context
- RISC-V context and open-source hardware
- SWOT analysis on RISC-V open-source hardware
- Conclusion

Toward the Software Defined Vehicle and hardware innovation

- **Impact of Centralized/Zonal architecture**
  - **High Performance Computer** architecture moves to scientific
    - Many core processors, **cluster organization**
    - AI accelerators and also crypto, communication and I/O
    - Computing efficiency and **energy consumption** via state and freq. control

- **Challenges to be solved** (ECS RIA[1])
  - Advanced computing, memory, and in-memory computing concepts
  - Novel devices and circuits that enable advanced functionality

- **Key Initiatives**
  - European Processor Initiative (EPI)
  - **RISC-V and Open-Source Hardware** as key ingredients



Unveiling the Transformation of Software-Defined Vehicles

[1] Electronic Components and Systems Strategic Research and Innovation Agenda, available at https://ecssria.eu/

A brief history

1990-2010: quasi-duopoly on instruction sets

2010: creation of the RISC-V ISA

Krste Asanovic

2016: SoftBank acquires ARM

2015: RISC-V Foundation

Since 2019: US/China trade wars

2020: NVidia attempts to buy ARM

2019: OpenHW Group

Since 2022: LLMs boom

2023: EU Chips Act

2023: RISC-V Software Ecosystem (Linux Foundation Europe)

IDM & geopolitical context

RISC-V ecosystem

RISC-V ecosystem

	Open-source solution examples	Commercial offer examples
Application	Application-specific software	
Operating system, libraries	Linux, FreeRTOS, Zephyr	VxWorks, QNX, PikeOS
Compilers, tools	GCC, clang/LLVM	IAR Workbench
Simulator / emulator	QEMU, Spike	AST/Vlab, Synopsis
Instruction set and extensions	RISC-V : a scalable family of ISA	
Core design	Berkeley Rocket, Boom, ETH PULP Western Digital SweRV Core	SiFive, XuanTie, Andes
IPs: memory controller, interconnect, GPU / NPU accelerators, peripherals	OpenWH Group labeled IPs	Synopsis, Arteris IP
Process design kit	Google Skywater PDK, eFabless	GlobalFoundries, TSMC
Foundry	*Not free & open-source !*	
SoC packaging		HiFive Freedom U540 SoC, Espressif ESP32-C

Open-Source Hardware and Business Model

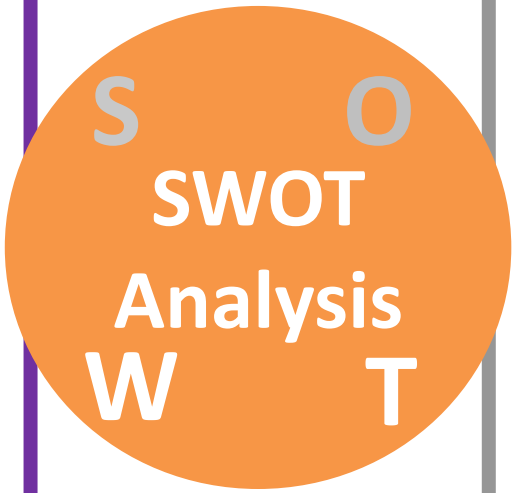
- Open-source hardware **to favor innovation and open collaboration**
  - **Inspiration from the success of open-source software**
  - Slow adoption due to current closed IP business model
  - **Only RISC-V ISA is open-source** and software tools (compilers, simulators..)
  - **RISC-V complete system is not open**
  - Some open-source RISC-V platforms exists (maturity, performance to be assessed)
  - EU found open-source collaborative project (Chips-JU umbrella)

- **New business model for hardware under maturation**
  - **Initiated by Academic and Industrial collaboration (3rd party funding)**
  - Next step Product-Service mix under progress with the **hypothesis of a dynamic ecosystem**
  - Then corporate competences (design, manufacturing, expertise) to be set-up
  - To reach platform model (membership, matchmaking) and distributed enterprise (license, certify)

SWOT on Open-Source Hardware

WEAKNESSES

- **Emerging RISC-V market**
  - Low penetration in automotive and IoT market
- **Reluctance of automotive industry players**
  - Open-source hardware is recent
  - Reliability and safety maturation needed
- **Current computing performance**
  - Gaps in current RISC-V performance
- **Non-standardized memory model**
  - Interconnect, cache, pipeline, optimization...
- **Maturity level on reliability**
  - IP/mechanism gaps for ASIL-D application
- **Incomplete solution for AI accelerators**
  - No GPU, NPU and gaps in SW toolchain
- **Risk on emerging solutions for HPC**
  - Geopolitical situation for CH and US



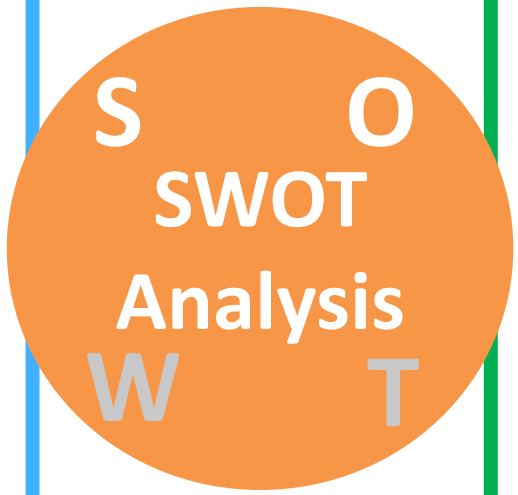
THREATS

- **Unclear business model for open hardware**
  - Complex, uncertain and not established
  - Liability issues
- **Competitiveness of EU**
  - R&D invest gap with CH & US (capital found)
- **Unbalanced public support in EU**
  - RISC-V is strategic for China
  - US pioneering and large company committed
- **Sovereignty for open source and ITAR rules**
  - Access of technology by CH (US Government)
- **Rare and valuable hardware skills**
  - High demand on talent with difficult recruiting
- **Security risk on open-source code**
  - Entry point for malicious code (Trojan)
  - To be balanced with mature automotive process

SWOT on Open-Source Hardware

STRENGTHS

- **Open hardware collaboration model**
  - share designs and resources
  - accelerates innovation through open collab.
- **Open marked for hardware accelerators**
  - Specialized IPs implementing instr. extension
- **Reinforce research and innovation**
  - free access to open resources facilitating experimentation.
  - Connecting to academic experts
- **Facilitate hardware-software co-design**
  - Adaptation and optimization with automation
- **Financial support from the EC and national bodies**
  - R&D initiatives: Chips-JU, EuroHPC, etc
- **EU Competence and IP Design ecosystem**
  - Fabless and SoC suppliers



OPPORTUNITIES

- **Diversification versus major semiconductor player**
  - Growing market of IA accelerators
- **Collaboration with China**
  - Numerous academic collaborations on HPC
- **Opportunities for French and EU Players**
  - Research Infrastructure and collaboration
  - Active IA, ioT, Cybersecurity market
- **Efficiency Brought by Technology**
  - Design small size CPU with power efficiency
- **Contribution of Safety knowledge expertise**
  - Differentiation in derived commercial solutions
- **Designing software stacks and tools**
  - Extension of freely available solutions
- **Chiplet as a catalyst for this technology**
  - Automotive industry is very active here

Conclusion

- **Open-source hardware**

  - Deploying RISC-V Core System and Accelerators

    € €

    - Enforce sovereignty and market resilience, mitigate **risk of concentration on single source**
    - **Enabler of commercial exploitation** issued from base impl. **on non-competitive topics**
    - **Opportunity for heterogeneous architecture** to meet the needs of embedded HPC for SDV

  - **Recommendation**
    - **Survey the RISC-V market** (very active)
    - Adopt a progressive approach based on **working groups to identify opportunities**
    - Engage automotive industrials in R&D **open ecosystem to accelerate maturation**
    - **Collaborate with academics to accelerate innovation**
    - **Healthy competition** on performance of core processing systems and accelerators
    - Get involved in standardization for the automotive sector

MOVING FORWARD TOGETHER*

**PROGRESSONS ENSEMBLE*

THANK YOU FOR YOUR ATTENTION

liliana.cucu@inria.fr

etienne.hamelin@cea.fr

philippe.cuenot@aumovio.com

The original white paper is available on SIA Website

Société des Ingénieurs de l'Automobile
2, rue de Presbourg • 75008 Cedex • France